Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-16. (Canceled)

17. (Currently Amended) A method of forming an integrated circuit package, comprising:

providing a package housing having a first plurality of bonding pads located on a first bond shelf, the first bond shelf including a top surface and a first edge;

forming a first conductive strip along the first edge of the first bond shelf, the first conductive strip wrapping around and over the first edge of the first bond shelf to electrically couple a first bonding pad of the first plurality of bonding pads on the first bond shelf to a first power bus under the first bond shelf; and,

forming a second conductive strip along the first edge of the first bond shelf, the second conductive strip wrapping around and over the first edge of the first bond shelf to electrically couple a second bonding pad of the first plurality of bonding pads on the first bond shelf to a second power bus under the first bond shelf, the second power bus having a voltage level less than the first power bus and located with the first power bus in a same horizontal plane of the integrated circuit package.

18. (Original) The method as recited in claim 17, wherein the first conductive strip is formed by plating a conductive material onto the first edge.

19. (Cancelled).

20. (Cancelled).

21. (Cancelled).

22. (Cancelled).

23. (Cancelled).

24. (Withdrawn) The method as recited in claim 17, wherein the package housing is provided by

forming a first conductive layer on a first dielectric substrate,

placing a second dielectric substrate on the first conductive layer of the first dielectric substrate, the second dielectric substrate having a second conductive layer, and

etching the second conductive layer to form the first plurality of bonding pads.

25. (Withdrawn) The method as recited in claim 24, wherein the first conductive layer forms the first conductor under the first bond shelf.

26. (Withdrawn) The method as recited in claim 24, wherein the etching of the second conductive layer to further form a second conductor, and the package housing has a second plurality of bonding pads located on a second bond shelf, the second bond shelf having a second edge, the package housing is further provided by

placing a third dielectric substrate on the second conductive layer of the second dielectric substrate, the third dielectric substrate having a third conductive layer, and

etching the third conductive layer to form a second plurality of bonding pads, and

the method further includes

forming a second conductive strip along the second edge of the second bond shelf, the second conductive strip wrapping around the second edge of the second bond shelf from at least one of the second plurality of bonding pads on the second bond shelf to the second conductor under the second bond shelf.

27. (Withdrawn) The method as recited in claim 26, wherein the second conductive layer forms the second conductor under the second bond shelf.

28. (Withdrawn) The method as recited in claim 26, wherein the second conductive strip is formed by plating a conductive material onto the second edge.

29. (Withdrawn) The method as recited in claim 26, wherein the second conductor under the second bond shelf is a power bus.

30. (Withdrawn) The method as recited in claim 26, wherein the second conductor under the second bond shelf is a routing trace.

31. (Currently Amended) A method of forming an integrated circuit package, comprising:

providing a package housing having a first bond shelf with a top surface and an inside surface;

forming a conductive material along the inside surface of the first bond shelf, a first portion of the conductive material wrapping around from the inside surface onto the top surface of the first bond shelf to form at least one of a ~~first~~ plurality of bonding pads on the top surface of the first bond shelf; and,

removing a second portion of the conductive material along the inside surface of the bond shelf to form a pair of separate conductive strips along the inside surface of the bond shelf with a first conductive strip of the pair of conductive strips coupled to a first bonding pad of the plurality of bonding pads coupled to a first power bus having a first voltage level and a second conductive strip of the pair of conductive strips coupled to a second bonding pad of the plurality of bonding pads coupled to a second power bus having a second voltage level less than the first voltage level, the first power bus and the second power bus are located in a same horizontal plane of the integrated circuit package.

32. (Original) The method as recited in claim 31, wherein the conductive material is formed along the inside surface by plating a conductive material onto the inside surface.

33. (Cancelled).

34. (Cancelled).

35. (Cancelled).

36. (Currently Amended) A method of forming an integrated circuit package, comprising:

providing a package housing having a rectangular bond shelf with a rectangular top surface and an inside surface perpendicular with the top surface, the bond shelf having a first plurality of bonding pads located on the top surface;

forming a conductive material along the side surface of the bond shelf, a first portion of the conductive material wrapping around from the inside surface onto the top surface of the bond shelf to couple to at least one of the ~~first~~ plurality of bonding pads on the top surface of the bond shelf; and,

removing a second portion of the conductive material along the inside surface of the bond shelf to form a pair of separate conductive strips along the inside surface of the bond shelf with a first conductive strip of the conductive material coupled to both a first bonding pad of the plurality of bonding pads and a first power bus having a first voltage level and a second conductive strip of the conductive material coupled to both a second bonding pad of the plurality of bonding pads and a second power bus having a second voltage level less than the first voltage level, the second power bus and the first power bus are located in a same horizontal plane of the integrated circuit package.

37. (Original) The method as recited in claim 36, wherein

the conductive material is formed along the inside surface by plating a conductive material onto the inside surface of the bond shelf.

38. (Cancelled).

39. (Cancelled).

40. (Cancelled).

41. (Previously Presented) The method of claim 17, wherein the forming of the first conductor strip and the forming of the second conductor strip comprises removing a portion of a conductive strip to separate portions of the conductive strip to form the first conductive strip and the second conductive strip.

42. (Previously Presented) The method of claim 17, wherein the first power bus and the second power bus are located within an identical horizontal plane of the package.

43. (Previously Presented) The method of claim 17, wherein the first power bus having a first voltage level greater than a voltage level of the second power bus.

44. (Previously Presented) The method of claim 43, wherein the first voltage level of the first power bus is substantially equal to 3.3 volts.

45. (Previously Presented) The method of claim 44, wherein the second voltage level of the second power bus is substantially equal to 2.0 volts.

46. (Cancelled).

47. (Previously Presented) The method of claim 31, wherein the first voltage level of the first power bus is greater than 3 volts.

48. (Cancelled).

49. (Previously Presented) The method of claim 36, wherein the second voltage level of the second power bus is 2 volts.